REMARKS

Claims 1-5 are pending in the application. Claims 1-2 are rejected under 35 U.S.C. § 102(b) as being anticipated by Song (U.S. Patent 5,539,467).

Claim 3 is rejected under 35 U.S.C. § 103 as being unpatentable over Song in view of Richards (U.S. Patent 5,392,071).

The above rejections are the same as those contained in the previous Office Action.

Claims 4 and 5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form.

Analysis of the Claim Rejection:

The Examiner has maintained the same rejections as in the previous Office Action. In response to the previous Office Action, it was argued that claims 1 and 2 are not anticipated by Song et al and that claim 3 is not unpatentable over Song et al and Richards et al at least because these references fail to teach or suggest the claimed B picture memory. The Examiner responds to that argument on page 2 of the present Office Action and provides various reasons why he believes Song et al stores B-pictures. Each of these reasons will be addressed individually.

First, the Examiner states that his citation of Fig. 5, element 52 as a B picture memory is legitimate because B pictures must be stored, otherwise the display of all the MPEG encoded pictures would not be possible without storing all the I, P and B pictures. Applicant respectfully disagrees.

Song et al inputs pictures in the order I, P, B1, B2, P2, B3, B4, and B3, and outputs pictures in the order I, B1, B2, P1, B3, B4, and P2 (see, for example, the top and bottom lines of

Figs. 4 and 6[1]). Accordingly, there is no need to store B pictures. For example, when the B1 frame is input to adder 56 of Fig. 5, the B1 data is added to the data of the I frame stored in frame memory 1 (element 45) and/or the P1 frame stored in frame memory 2 (element 46). The data output by adder 56 is directly applied to multiplexor 59 for outputting to the image processor. That is, when the B1 frame data is input, B1 frame data is output at the same time, as shown in the charts of Figs. 4 and 6. It is not necessary that the B pictures be stored.

Second, the Examiner states that Song's Fig. 5, element 52 is a bi-directional latch for a temporary storage unit for temporarily storing bi-directional pictures. Applicant respectfully disagrees with this statement because the bi-directional latches 52 and 53 merely allow the passage of data in two directions. This is an entirely different concept from the bi-directional picture (i.e., B picture) of the MPEG system, where a bi-directional picture is coded/encoded with respect to previous and future pictures.

The Examiner further states that in Song's Fig. 5, element 55 can produce the B-frame image data and send it to element 57, a FIFO memory or a first-in-first-out memory for temporarily storing the B-frame image date before displaying the MPEG decoded pictures. Applicant respectfully disagrees with the Examiner's analysis because there is no teaching or suggestion in Song et al that the FIFO memory 57 of Fig. 5 stores a B-frame. As shown in the timing diagram of Fig. 6, FIFO writes only the I-frame, the P1-frame, the P2-frame, and the P3-frame. Further, as explained above, Fig. 6 indicates that B-frame data is output at the same time that it is input. This is consistent with the explanation of the operation of the Fig. 5 device in col. 10 of Song et al.

Lastly, the Examiner states that element 79 of Fig. 7 is also considered a B-frame buffer that stores a B-frame signal. However, the buffer 79 is merely a 3-state buffer as described, for example, on pages 424-425 of the book "Fundamentals of Logic Design". Enclosed are pages

[1] Applicant suspects there is a typographic error in the bottom line of Fig. 6, where the entry "RP1" should be--B1--.

424 and 425 which describe the 3-state buffer which is used as an interface between two circuits, but does not act to store data.

In view of the comments above, Applicant submits that Song et al does not teach or suggest a memory for storing B-pictures.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

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